VIVA DATE : 29.10.2012

Candidate: Ms.S. Hemachitra **Guide: Dr.A.Kandaswamy**

CERTAIN DESIGN AND MODELING APPROACHES FOR RUNTIME RECONFIGURABLE COMMUNICATION ARCHITECTURES FOR SYSTEM ON CHIP

System-on-Chip (SoC) is the integration of all the necessary electronic circuits of diverse functions onto a single chip to evolve as a complete electronic system that performs the more complex and more useful final product function. Usually, SoC designs consume less power, have low cost and high reliability. A typical SoC consists of one or more microprocessors, memory blocks, timing sources, peripherals, external interfaces, analog interfaces, voltage regulators, and power management circuits. A communication architecture (CA) is used to transfer data between different SoC components. Therefore, the performance of the SoC depends upon the efficiency of CA. As VLSI design technology is getting more communication centric rather than computation centric, there is a necessity for the on-chip CAs to work efficiently. The on-chip buses are the more commonly used CAs. Some of the bus standards available are AMBA, Wishbone, IBM Coreconnect, Sonics SMART Interconnect, etc.

In order to implement complex SoC designs, the statically configured CAs are no longer suitable. The CAs should possess some dynamic reconfigurability features which means, some of its communication protocol parameters adapt to changing traffic patterns and needs of the system during execution i.e. at run time and can result in better optimization of design goals of power and performance. Most state-of-the-art CAs provide only limited and static configurability features. Therefore, this research is aimed at incorporating dynamic reconfigurability feature in some of the existing on-chip communication architectures by changing the protocol parameters, either the arbitration scheme or topology of the CA dynamically.

Lottery algorithm is a popularly used arbitration algorithm in Shared bus. The existing lottery algorithms have the disadvantages like large average latency and high cell loss factor. In the proposed Integrated Dynamic Adaptive Lottery (IDAL) arbitration algorithm, the ticket allocation and ticket refreshment processes are done automatically at runtime. Therefore, in the proposed IDAL algorithm the Average Latency is reduced by a maximum of 33.33% and Cell Loss is also reduced. A performance analysis of the IDAL algorithm with respect to changes in the parameters like refresh rate, traffic type, and buffer size is done. The optimal values of the three performance parameters are derived during the analysis. Thus, the IDAL algorithm could be used for bus arbitration in SoC design over the other existing arbitration algorithms.

The main problem of Shared bus is low scalability. SAMBA bus attempts to overcome the scalability problem of Shared bus. It is capable of delivering multiple transactions in one bus cycle.

In SAMBA bus, multiple overlapping transactions cannot be performed simultaneously. So, in this work, two dynamically reconfigurable SAMBA bus architectures are proposed to improve SAMBA bus. Both the proposed architectures reconfigure their topology at run time and enable multiple overlapping transactions to be performed simultaneously. Simulation results show an increase in bandwidth, scalability, and reduction in average communication delay (about 58.4%) for both the architectures. The two proposed architectures are well suited for high speed real time applications due to the above mentioned advantages.

Shared buses have larger wire and load capacitance which results in larger power consumption and longer data transfer delay. Segmentation of bus allows parallel data transfers on different segments and allows selective shutdown of unused bus segments which improves performance and saves power respectively.

The existing segmented bus architecture has two main limitations namely, high intersegment data transfer delay and high arbitration delay. Two dynamically reconfigurable Segmented bus architectures are proposed in this work. Both the proposed architectures reconfigure their topology at run time so as to overcome the limitations mentioned. Simulation results show increased speed (by 20%), improved bandwidth, improved scalability, and reduction in average communication delay without any area and power overhead. Therefore, the two proposed architectures seem to be highly efficient and hence, they can be used in high speed SoC applications.

On-chip buses have low complexity and standardized communication protocols. But the limitations are low scalability, limited concurrent communication capability, long wiring delays, and limited bandwidth regulation characteristics. The Network-on-Chip (NoC) approach adopts the conventional network techniques for on-chip communication leading to better performance. In SoC designs where the number of components is high, NoC approach is advantageous.

In this work, a reconfigurable SDM based NoC router is proposed. During runtime, the proposed NoC router can reconfigure either Mesh topology or Benes topology for data transfer between source and destination nodes. Simulation results show that SDM routers are more efficient than TDM routers in terms of power consumption and speed. Area, Power, Delay, Logic Utilization and I/O Buffer Utilization of the proposed NoC router is obtained from the simulation results. The working of the proposed NoC router is verified using bit streams, audio data, and image data. Therefore, the proposed NoC router can be a means of providing scalable on-chip interconnects for SoC designs and can lead to better performance and more efficient utilization of on-chip resources.