ABSTRACT

A Cochlear Implant (CI) is a surgically implanted electronic device that provides a sense of sound to a person who is profoundly deaf or severely hard of hearing. Unlike hearing aids, the CI does not amplify sound, but works directly stimulating any functioning auditory nerves inside the cochlea with electric fields stimulated through electric impulses. The speech processor splits the auditory signal into bands of different frequencies and converts them into suitable codes for stimulating the electrodes implanted in the cochlea of the ear. The electrode activates auditory nerve fibres to provide hearing sensation. For the economical less affluent people with hearing ailment, it may be too costly to afford for this equipment to recover from the hearing loss. The cost reduction may be achieved with reduced area, low power and enhanced performance of the CI. This objective intuited both the analog and the digital based CI designers to research their methods to provide people with cheaper and highly intelligible CI.

The speech processor for the CI is designed and implemented both in analog and digital domain. In analog domain, circuits are vulnerable to temperature changes and causes abnormal conditions which will not solve the problem for CI users. Whereas the speech processor designed in digital domain are robust, but there will be trade-off with more area. This trade-off is decreased to an acceptable level using algorithm to architectural transforms of Very Large Scale Integration Digital Signal Processing (VLSI DSP). The function of speech processor is implemented with suitable algorithms like Continuous Interleaved Sampling (CIS), Spectral PEAK (SPEAK), Advanced

Combination Encoder (ACE), Spectral Maxima Sound Processor (SMSP) and few more. Among these speech processing algorithms, CIS is the most common and famous algorithm used by many manufacturers of CI. In this algorithm splitting of speech signal into bands of frequencies is implemented by filter bank approach and Fast Fourier Tranform (FFT) approach. This work deals with design and implementation of filter bank using VLSI DSP to obtain low area, low power and high speed speech processor for CI.

The auditory filters of CIS are implemented as a narrow band pass filters which are realised as Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters. Higher order FIR requires more memory to store its coefficient values so the area occupied by these filter becomes more. XSG tool provides Distributed Arithmetic (DA) FIR compiler block that represents the single FIR band pass filter of order 877 and targets the dedicated hardware resources in the FPGA boards to create highly optimized implementations. DA FIR blocks are used to implement 16 channel filter bank to split input speech spectrum into different frequency bands.

According to CIS algorithm of speech processor the signal energy extracted from the output of these filter banks are converted to stimulating pulse that excites the micro electrodes inside the ear to stimulate the auditory nerve. XSG based DA FIR filter bank proves that design, analysis and testing of the filter with real time signal is made possible in less time. FIR based filter banks used 100% of available resources on Virtex II Pro board and 41 % of available resources on Virtex 7 board.

mimicking the bionic ear, the eighth order IIR filter realization is used. The high performance of this filter is accomplished by using highly efficient adders, multipliers and appropriate delays. In order to minimize the power consumption due to huge adder circuitry, ripple carry adder is used here to provide less power consumption. Simulation results show that the area and power consumption of the designed filter are $0.105mm^2$ and $760\mu w$ respectively.

The next work in this study proposes the folded architecture for the same eighth order IIR realization of GTF. Folding algorithm is applied to the second order digital GTF which reduces the number of multipliers from five to one and the number of adders from three to one in the design without changing the characteristics of the filter. Folded second order filter sections is cascaded with three similar structures to realize the eighth order digital GTF whose response is a close match to human cochlea response. The silicon area is reduced from twenty to four multipliers and twelve to four adders using the folding architecture. A new multiplier is proposed based on the Canonical Signed Digit (CSD) representation of the input samples and the coefficients. In the folded architecture instead of conventional multiplier,

The last work in the study proposes a Fractional Delay (FD) FIR filter for a directional speech enhancement based on the dual microphones of the CI developed to improve speech recognition. A technique called delay sum beam forming, which requires a specified delay to be offered to the signal coming from one of the two microphones is used. The need for FD filter arises here to provide the specified FD. The proposed work involves the design of maximally flat Fixed Fractional Delay (FFD) FIR filter and Variable Fractional Delay (VFD) FIR filter using the CSD multiplier which uses the numerical strength reduction technique to reduce the area occupied and the power consumed and enhances the speed of operation. It is found that maximally flat FFD FIR produced a fractional delay of 1.427 samples (x(n-1.427)) instead of x(n-1) when the distance between two microphone is 0.01m and the system clock period is 22.7 μs whereas VFD FIR produced FD of only 1.4 samples for the same specifications. With maximally flat FFD FIR filter, CSD based FFD FIR has 35% less area and 96.67% less power consumption with 5% increase in speed with respect to conventional direct form FFD FIR filter.