ABSTRACT

Design of digital VLSI circuits entails many challenges as a consequence of rapid growth of semiconductor manufacturing technology and the extraordinary levels of design complexity and the gigahertz range of operating frequencies. These challenges include keeping the power dissipation within acceptable limits. The remarkable reduction in transistor size and the subsequent increase in the more number of devices on a single chip, in combination with the budding demand for portable devices, increases the power consumption which lead to major challenge in Very Large Scale Integration (VLSI) circuit design and testing. So we need to minimize power dissipation in circuits which requires accurate estimation of the dissipated power during the design phase. This helps in avoiding complicated and expensive redesign that might be required due to power constraint violations. This thesis proposes techniques to overcome these challenges during design and test.

A Power estimation method for Complementary Metal Oxide Semiconductor (CMOS) VLSI circuits using Back Propagation Neural Network (BPNN) is proposed. Motivation of this work is to develop an automated power estimation techniques for CMOS VLSI circuits using statistical tools like BPNN. It overcomes the disadvantages of power estimation by simulating complex circuits using power simulators. Regression analysis and Mean Square Error analysis is performed to measure the deviation of estimated power from that of actual power results obtained through SPICE/Monte Carlo simulations. The deviations from ideal power estimator for NAND and NOR based combinational circuits is using BPNN about 0.77% and 1.04% respectively and for sequential circuits it is about 0.01%. The Mean Square Error (MSE) reported for NAND and NOR based combinational circuit is 0.88751 and 1.08402 and for sequential circuits it is about 6.254×10^{-05}. The result shows that BPNN based method estimates power precisely.

The next proposed work employs an Adaptive Neuro Fuzzy Inference System (ANFIS) that is capable of estimating the power precisely for the CMOS VLSI circuits, without the knowledge on actual circuit structures and interconnections. ANFIS applied to power estimation application is relatively new. The experimental results show that ANFIS with hybrid optimization employing linear method produces better results in terms of minimal testing error which varies from 0 % to 0.86 % which is less when compared to BPNN. Hence, ANFIS with exclusive characteristics appears as a better choice for estimation of power in CMOS VLSI circuits. ANFIS has a low RMSE of 0.0002075 and high coefficient of determination of 0.99961 for power estimation. From the result obtained it is concluded that ANFIS based power estimation is more precise than BPNN based power estimation.

A Modified Low Transition LFSR (MLT LFSR), Tversky Index counter and Low Transition Test Pattern Generator (LT TPG) has been proposed for test power minimization in CMOS VLSI circuits.

A MLT LFSR based test pattern generator is proposed, in which consecutive test vectors are compared. When there is a transition between corresponding bit pattern, a new intermediate pattern is inserted by generating a random bit and positioning it in the corresponding bit of change from either first or second half of LFSR. The advantage of our proposed technique is without affecting the randomness, transitions between patterns is reduced. The reduction in switching activity is about 34% when compared to existing LTLFSR. Power consumption is reduced up to a maximum of 8.7%, 18.2% and 36.2% with respect to Low Transition LFSR (LTLFSR), Multiple Single Input Change (MSIC) test pattern generator and LFSR based testing of ISCAS'85 combinational circuits. Testing of ISCAS'89 Benchmark sequential circuits using proposed MLTLFSR provides a maximum power reduction of up to 3.2%, 1.3% and 10% respectively when compared with LT

LFSR, MSIC and LFSR techniques. Fault coverage is maintained in the range of 90% to 100% with a marginal increase in area overhead.

A test vector reordering has been performed using distance measures. The distance between the test vectors are calculated using Hamming, Gray code and Tversky index, an adjacency matrix is formed and reordering is performed. If the test vectors applied to Circuit Under Test is not optimized, for minimum switching activity power consumption will increase, this can be reduced by increasing the correlation. The experimental results for combinational circuits show that the Tversky index based reordering, reduces the switching activity up to a maximum of 51.8% when compared with other existing distance measures. The power consumption is found to be 48 % lesser than that of other distance based reordering techniques.

A low transition test pattern generator (LTTPG) is proposed. The proposed LT TPG generates a test sequence with minimum switching activity by means of increasing the correlation among test vectors by bit XOR ing the outputs of binary ripple counter with a constant seed. The minimum transition test sequences are accomplished by an efficient utilization of XOR gates in appropriate locations. Experimental results for ISCAS'85 benchmark circuits shows up to a maximum of 79% and 92% reduction in power when compared with MSIC and LFSR respectively. Proposed method on ISCAS'89 gives power reduction of 65.5% when compared to MSIC technique.

The simulation results show that for CMOS VLSI circuits, the proposed BPNN and ANFIS techniques estimate power precisely at design phase and test pattern generators using MLTLFSR, LTTPG and tversky index counter optimize power during testing phase effectively.