ABSTRACT

In recent times, the development of wideband wireless communication system has been increased due to customer interest towards high-speed wireless communication, Orthogonal Frequency Division Multiplexing (OFDM) transceiver design is a pivotal task. The OFDM transceiver used to increase the data transmission faster by excellence of its Multi-carrier modulation and targets high spectral efficiency. The Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT) algorithms play a vital role in OFDM system, which requires more hardware complexity. The structure of FFT processor depends on the selection of radix algorithms. The choice of small radix in the FFT processor results in simple butterfly structures. Meanwhile the numbers of twiddle factor multiplications are reduced using higher radix values. Hence, in FFT processors, Multi-radix algorithms are desirable to minimize the hardware complexity.

An improved area and power efficient FFT/IFFT processor is proposed for OFDM transceiver. In the proposed work, a radix-2^5algorithm based 512-point FFT/IFFT Processor having Multi-path delay structure with eight parallel data-paths is considered for implementation. Multiplier is an important component in FFT processors, which consumes more hardware area. Vedic multiplier based FFT/IFFT processor helps to implement an area and power efficient architecture. The existing multipliers used in the FFT/IFFT processor occupy more hardware. Urdhva Tiryakbhyam (Vertical and Crosswire) Vedic mathematical sutra is used in the proposed FFT processor, which helps to reduce hardware complexity. It eliminates redundant multiplications steps and decreases gate delay. The twiddle factor

multiplications in the FFT architecture are calculated using 16-bit Vedic multipliers. In addition, carry save adders and compressor adders are used in Vedic multipliers to reduce the carry delay and area.

The carry save adder based Vedic multiplier used in 512-point FFT processor occupies 163K gates and 73.6 mW of power consumption. The layout core area for the FFT architecture is 0.53 mm^2. The throughput rate of FFT structure has increased to 2.72 GS/s at 340 MHz. Compressor adder based Vedic multiplier used in FFT processor occupies 148K gates and 67.4 mW of power consumption. The proposed FFT achieves maximum clock frequency of 368.87 MHz with throughput rate of 2.95 GS/s. The Vedic multiplier based FFT processor has a reduced gate count of 48.9%. It also achieves reduced power consumption in the range of 34% to 21% compared to the existing FFT processor. The compressor adder based Vedic multiplier provides 9.2% reduction in total gate count and 8.4% reduction in power consumption compared to carry save adder. Hence, Vedic multiplier based compressor adder can be employed in FFT processor.

In an OFDM system, orthogonal subcarriers offer narrow bandwidth. The subcarriers in OFDM are transmitted using different modulation techniques like 16-QAM, QPSK, OQPSK and BPSK. The 16-Quadrature Amplitude Modulation (16-QAM) is an efficient modulation technique, carries data on amplitude and phase. It is a preferred digital modulation method in wireless communication, which reduces bit errors and noise effects during data transmission. There are 16-symbols in QAM and each symbol consists of two bits I and Q components. The 16-QAM design has 4 amplitudes and 12 phases. The discrete amplitudes ±3 and ±1 are used in 16-QAM design. The proposed 16-QAM architecture is transmitted over different input bit patterns (8, 16, 32 and 64) and modulated by variable clock frequencies (1.2 KHz to 19.2 KHz).

The compressor adder based Vedic multiplier used in 16-QAM transceiver design provides an area efficient architecture. The proposed design is implemented using Virtex 4 XC4VLX100 -10 ff 1148 FPGA device occupies 706 slices and 1280 4-input LUTs. The 16-QAM design occupies 77K gates and operates with maximum clock frequency of 99.37 MHz. The compressor adder based Vedic multiplier used in 16-QAM design has reduced slices of 75% and a reduced 4-input LUTs of 72% compared to the existing 16-QAM design. The 16-QAM is also implemented using Spartan-3 XC3S200-5 pq208 FPGA device occupies 593 slices and 1093 4-input LUTs. The 16-QAM uses Vedic multiplier has reduced slices in the range of 80 % to 27% as compared to the existing 16-QAM design. It also achieved a reduced 4-input LUTs in the range of 76.6% to 6%. The 16-QAM transceiver design uses Vedic multiplier for implementing an area efficient architecture.

The OFDM transceiver transmits subcarriers with orthogonal frequencies for high-speed data transmission. The proposed OFDM transceiver is transmitted over different input bit patterns (64, 128) and subcarriers modulated by orthogonal frequencies (1.2 KHz to 19.2 KHz) for saving the bandwidth in data transmission. The OFDM system is constructed by 64-subcarriers in parallel transmission and it is modulated by several modulation schemes like 16 QAM, QPSK, OQPSK and BPSK. To scale down the complexity of the twiddle factor multiplications in FFT blocks the radix-2^2, radix-2^3, and radix-2^4 are considered. Urdhva Tiryakbhyam Vedic multiplier introduced in the FFT/IFFT processor reduces undesirable multiplications and generates partial products. The compressor adders help to add the partial products in the Vedic multiplier.

The Multi-radix FFT blocks use 90 nm CMOS technology with 0.9 V supply voltage in the OFDM transceiver implementation. The FFT processor has a core area of 0.47 mm^2 and throughput of 162 MS/s at

162 MHz. It also occupies 21K gates and 5.21 mW power consumption. The proposed FFT algorithm has reduced gate count in the range of 37% to 25% compared to the existing processor. It also achieved reduced power consumption in the range of 46.6% to 33.9%. The proposed Multi-radix FFT processor occupies less area and consumes minimum power. Thus, an area efficient architecture is possible for OFDM system using Vedic multiplier based Multi-radix FFT processor.

The proposed OFDM transceiver implemented using Xilinx Virtex 2 XC2VP 500 -6 fg256 FPGA board occupies 52.4K gates, 64 mW power consumption and 751 slices. The OFDM system has reduced slices in the range of 71% to 47% compared to the OFDM system. From the simulation results, it can be found that the area of proposed OFDM system is considerably less. Hence, the compressor adder based Vedic multiplier used in FFT/IFFT processor proves to be the promising candidate in OFDM transceiver to achieve high area efficiency.