ABSTRACT

In recent years, the mobile communication market has been growing rapidly. Frequency Synthesis, clock and data recovery, amplitude and frequency demodulation, etc. are the major roles of Phase Locked Loop (PLL) in mobile communication. One of the challenges in PLL design is reducing the acquisition time, the time needed for a PLL to lock to the frequency and phase of a harmonic reference. The faster a PLL can acquire lock to a new frequency, the faster the system can be made to operate. Designing a frequency synthesizer having low settling time is a challenge in the mixed-signal circuit design area. The Phase Frequency Detector (PFD) and Charge Pump (CP) are the major blocks of a Charge Pump PLL (CP-PLL) which decides it's settling time. The magnitude of frequency step of a PFD decides the settling time of a PLL. Larger the frequency step, less will be the settling time of the PLL. The CP should be able to handle these large frequency steps for the proper operation of the PLL. Hence PFD and CP are chosen as the domain of present research work. In this work, the methods to improve the performance characteristics of PFD and CP are proposed and the outcome is analysed.

The two important factors that affect the characteristics of a PFD are dead-zone and blind-zone. A dead-zone occurs when the phase difference between the two input signals is very close to 0^0 and the small phase difference cannot be detected by the PFD. The blind-zone problem occurs when the phase difference of two input signals becomes $\pm 2\pi$ radians. The dynamic logic PFD is dead-zone free due to the inherent characteristic of the logic, but blind-zone problem still prevails. The reason for blind-zone is the insensitive of the PLL to any transition of the input signal during the reset phase. As the PFD cannot detect the rising edge of the leading signal during the reset phase, it will wrongly interpret that the leading signal is lagging and vice-versa. The blind-zone is the major factor that limits the detection range of PFDs and may deteriorate the PLL locking characteristics. In this work, different techniques are employed for reducing the blind-zone and hence increase the detection range of the PFD.

Current leakage and timing and current mismatches are the basic non-ideal effects of a CP. Charge injection, charge sharing and clock feed-through are the main sources of leakage current. Current leakage can be avoided to an extent by choosing switch at source architecture for CP circuit. Timing mismatch is due to the fact that the UP signal should be inverted before applying to the PMOS switch and this causes an inverter delay between the UP and DN signals. The reason for current mismatch are, the difference in mobility of electrons and holes and the limited output

impedance of the CP circuit. In this work, the output impedance of the CP circuit is increased to achieve current matching.

In order to increase the detection range of a PFD, its reset time is to be decreased. Once the reset time is reduced to its maximum limit, pre-charge time occupies the major portion of the blind zone and so it should be reduced. The techniques used for increasing the detection range of PFD are inverter sizing, transistor reordering and use of pre-charge transistors.

During the reset operation, the PFD is considered as cascade connection of three inverter stages. So by proper inverter sizing, the inverter delay is reduced. The next step is the modification of the circuit architecture to reduce the signal path length. By interchanging the NMOS transistors in the second stage inverter of the PFD, the extra resistance and capacitance of one transistor is bypassed and the signal path length is reduced. This reduces the reset time of PFD. The introduction of pre-charge transistors driven by the direct input signal aids in faster pre-charging of the internal nodes of the PFD. These three techniques decreases the reset time and blind-zone and hence increase the detection range of the PFD.

The output current mismatch in the existing CP circuit is minimized by increasing the output impedance of the circuit. The use of high compliance cascode current mirror and Gain Boosting Amplifier (GBA) are employed in the output side of CP circuit to obtain high output impedance.

The output impedance of cascode current mirror configuration is very high compared with its counterparts. The significance of high compliance cascode current mirror over simple cascode current mirror is that it provides current matching along with high output impedance. With the help of GBA, the output impedance of a CP is further increased. The GBA multiplies the transconductance of the main amplifier by a factor 'A' and the resultant output impedance will be Ag_mr_o instead of g_mr_o. The idea is to keep the drain-source voltage of the amplifying transistor constant, by a negative feedback amplifier.

All the circuits are simulated with 500 MHz input signals using Cadence SpectreRF simulator in UMC 180 nm technology with a supply voltage of 1.8 V. In the proposed PFD, reordering of the inverter sized PFD along with the addition of pre-charge transistors aided in 17.83% reduction of the reset time. The reduction in reset time resulted in the reduction of the blind-zone and hence the detection range of the PFD is increased. The usage of high compliance cascode current mirror and GBA achieved excellent current matching for the proposed CP. For the proposed CP, the maximum difference between the IUP and IDN currents is less than 0.1%. The proposed high output impedance CP compensates for the current mismatch problem in CP. Thus a PLL with fast settling time can be obtained.