ABSTRACT

Very Large Scale Integration (VLSI) technology is a major milestone in the development of solid state electronics. The advancement in VLSI technology has allowed the integration of more and more functionalities into a single chip. The chip density, physical design, fabrication and testing complexity have therefore increased exponentially. Hence testing of VLSI circuits plays a key role in the design flow and has become a challenging task for design and test engineers. When the chip density was less, majority of the faults were single stuck-at faults and hence this model was sufficient to model all the faults. However with increased chip density, this may not be the case. Recent empirical data from a real-life design environment for 453 failing devices show that 41% of the defects found cannot be modeled with a single fault. Additionally, 22% of the remaining 59% defect cases cannot be modeled using the single stuck-at fault model. Therefore, in more than 60% of the cases where a chip is returned for defect analysis, multiple stuck-at fault diagnosis is required and the classical single stuck-at fault model may be inadequate (Liu and Veneris 2005). In a circuit with ‘n’ lines, there are around 3^n-1 multiple stuck-at faults when compared to 2n single stuck-at faults. This again posed a problem because a large number of faults involve a large search space. This problem of large search space combined with the problem of storing huge data from the fault simulator made test pattern generation for multiple stuck-at faults a challenging task.

Test Pattern Generation (TPG) techniques for multiple stuck- at faults together with test pattern reduction algorithms are proposed and analyzed in this thesis for minimizing the power dissipation during testing of VLSI circuits. Genetic Algorithms (GA), Modified Particle Swarm Optimization (MPSO) and Zero Suppressed Binary Decision diagrams (ZBDD) are the techniques employed for test pattern generation while test pattern reordering algorithm and don't-care filling algorithm are the techniques used for test power reduction.

The first significant contribution to the thesis uses genetic algorithms to generate the test patterns for the multiple stuck-at faults injected into the circuit. This method was implemented and simulated on ISCAS 85 and ISCAS 89 circuits. The switching activity due to the transitions between the test patterns obtained from this method, when applied as inputs to the Circuit Under Test (CUT) was estimated and the Average Switching Activity (ASA) was calculated.

The second significant work proposed is a test pattern generation technique for the multiple stuck-at faults using a Modified Particle Swarm Optimization (MPSO) algorithm. The switching activity due to the transitions between the test patterns, when applied to the CUT was observed and the ASA was calculated. It was found that the MPSO based test pattern generation had a reduced ASA as compared to that of GA.

The third work given in the thesis is a reordering algorithm used to rearrange the test patterns applied to it so as to reduce the number of

transitions and hence the power. As the test patterns obtained by MPSO had lesser transitions when compared to that of GA, these test patterns were applied to a reordering algorithm to further reduce the power. The test patterns obtained in MPSO were fully specified with only 0s and 1s. The test patterns obtained are reordered based on the functional distance between the test patterns and also based on the internal switching activity among these patterns. It was observed that the ASA gets considerably reduced after reordering, when compared to that before reordering.

The fourth work involves a test pattern generation technique for the multiple stuck-at faults using a Zero Suppressed Binary Decision diagram (ZBDD) approach. The test patterns obtained by this method were not completely specified and had don’t-cares in addition to 0s and 1s. By proper filling these don’t-cares using don’t-care filling techniques, the transitions between the patterns obtained by this method were reduced and it was found that the ZBDD based method of test pattern generation had a lesser ASA as compared to that of GA and MPSO.