ABSTRACT

With each new CMOS technology generation, the functional correctness of the design and design parameters become more sensitive to the increasing subthreshold leakage current and circuit parametric variations. These variations in process parameters severely affect the minimum geometry transistors commonly used in area constrained circuits such as Static Random Access Memory (SRAM) cells. The device parameters translate into variations in circuit parameters like leakage of power, leading to loss in parametric yield. These deep sub-micron effects, if not considered, results in design with poor yield. Hence, there are several design challenges for nanometer SRAM design. To deal with these design challenges, it is important to give emphasis on leakage power reduction, fault modeling, structural testing, Design For Test (DFT) techniques and self repairable architectures to ensure and maintain test cost effectiveness and low defect levels.

There are several low-power circuit-design techniques to achieve low-power and low-voltage SRAM design. Dynamically lowering power supply and biasing techniques such as body biasing and source biasing during standby mode remains the most effective ways to achieve low-power consumption. However, supply-voltage reduction and biasing techniques increase the failure rate of stored data. Thus, leakage power reduction is achieved at the cost of lower data-reliability.

Stored SRAM cell data faces the following failure mechanisms

- Parametric failures like read upset, access time failure, hold failure and write failure due to process parameter variations.
- Soft errors due to cosmic particles or alpha particles from die packaging.
- Poor data stability due to supply voltage reduction to meet low power constraints.
- Data retention fault due to source biasing for leakage power reduction.

Hence the thesis focuses on improving the performance of SRAM design by reducing the power consumption. A Novel 9T SRAM cell is proposed, to improve the data stability, by completely isolating the bit lines from the data storage nodes during read operation. This isolation prevents the rising of the node voltages storing '0' from ground level, thus increasing the read stability of the proposed 9T SRAM cell. The dynamic power is reduced by utilizing only one bit line (BL) for charging/discharging during the write operation.

But as technology scales down, leakage power dominates the dynamic power consumption. Hence a DFT is proposed to reduce the leakage power consumption using source biasing and supply voltage scaling. At standby mode, when the sources of NMOS transistors are biased, the leakage power

gets reduced. Lowering the supply voltage is another technique to reduce the leakage power. But both the techniques results in the occurrence of hold failure. The DFT proposed, reduces the probability of occurrence of hold failure, by generating an optimized source bias voltage and minimum supply voltage to be applied to SRAM array. But inspite of the applied voltage, the hold failure still exists at nanometer design. The principal reason for hold failure in SRAM cell is the variation in threshold voltage due to random fluctuation of dopant atoms.

Hence a DFT is proposed for nanoscale SRAM. It identifies the presence of weak cells in SRAM array responsible for hold failures with minimum test time. The source bias voltage is applied and SRAM array is monitored for hold failures using March test. The cells affected due to hold failures are replaced using redundant columns in the SRAM array during testing. If the number of March tests is more, the test time also increases accordingly. The DFT proposed, reduces the number of March tests by predicting the initial source bias voltage using V_{SB} predictor. The V_{SB} is predicted based on the presence of weak cells in array, which are responsible for the hold failures. Thus, with the predicted V_{SB} as initial V_{SB} applied to the SRAM array, maximum V_{SB} is determined with maximum of two March tests. Hence, the total test time is reduced. Moreover, the time taken to predict the initial $V_{SB,}$ is independent of the size of the SRAM array because all the cells in an array are accessed at the same time to perform the write operation followed by the read operation to determine the weak cells. The result shows

that the proposed DFT is able to reduce the leakage power for nanoscale SRAM with minimum test time as compared to the existing technique.

Another major barrier that the CMOS devices face at nanometer scale is increasing process parameter variations. Variations in the process parameter results in functional failures such as read, write, access and hold failures in SRAM. If the variations in process parameters, in particular threshold voltage are prevented, then the probability of occurrence of functional failures can be avoided. Hence a self repairable architecture capable of identifying the SRAM array with low and high V_t transistors by monitoring the leakage current of the SRAM array is proposed. It utilizes Adaptive Body Bias (ABB) technique, as an adaptive repair technique. By applying Reverse Body Bias (RBB) to low V_t transistors, their V_t increases thereby reducing read and hold failures in SRAM cells. Similarly, application of Forward Body Bias (FBB) to high V_t transistors decreases their V_t, which reduces the access and write failures in the SRAM cells. However the range of high V_t transistors is more making it difficult to bring the entire range to nominal V_t range by applying a single forward body bias voltage. Hence the high V_t zone transistors are divided into two different zones and accordingly two different forward body bias voltages are applied. The result shows that the proposed architecture is able to reduce the amount of deviation of high V_t values from nominal V_t values as compared to existing technique. This results in a highly reliable self repairable architecture as compared to the existing architectures.

The defects occurring in SRAM due to process parameter variations are conventionally detected using March algorithm. March algorithm has a

time complexity of O(n), where n is the number of bits in the SRAM array. Hence, as the density of memory increases, the test time for March algorithm also increases. An efficient and economical memory test should provide the best fault coverage in the shortest test time. Besides the fault detection, manufacturing memory tests must also include a diagnostic capability that allows identification and possibly repair defective locations by applying redundant elements.

Hence a Built In Self Repair (BISR) architecture is proposed, which has Built In Self Test (BIST) and Built In Redundancy Analysis (BIRA) modules. The BIST utilizes transient current testing method for fault detection in SRAM array. This reduces the test time complexity by 50% as compared to March test for fault detection. BIRA module executes the proposed redundancy analysis algorithm for SRAM. The algorithm repairs two or more consecutive damaged lines with spare rows. By implementing redirection of the faulty row to the next available word line address, wire interconnect delay is minimized. It significantly reduces the access time penalty compared to the case of redirecting to the redundant rows. The repair of the faulty cells with spare row is done by BIRA module during chip reset. Hence, no extra power due to BISR is consumed during normal operation

Technology scaling also increases the sensitivity of SRAM devices to radiation. Many of the radiation induced events create electron-hole pairs that upset the storage nodes of SRAM cells. The ionizing particle hit on the SRAM cell can happen, at any instant of time. Hence a Built In Current Sensor (BICS) is proposed capable of detecting soft errors during standby

mode and operating mode. It has a ‘1’ to ‘0’ flip detector and ‘0’ to ‘1’ flip detector which detects and amplifies a transient current pulse generated due to the flip and provides logic level voltage pulse. This voltage pulse is fed to the asynchronous latch that generates the error signal. To enable the BICS operation under operating condition of SRAM, the logic circuitry with delay element is used. This circuit is used to control the reset signal for all operating conditions. The result shows that the proposed BICS is capable of detecting soft errors both at standby and operating modes.